



#4-10-01
2812

IN THE UNITED STATES
PATENT AND TRADEMARK OFFICE

PATENT APPLICATION

Sailesh Chittipeddi

CASE 79

Serial No. 09/596,382

Filed 06/16/2000

Title Process For Manufacturing An Integrated Circuit Including A Dual-Damascene Structure And A Capacitor

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

Attention: Office Draftsman

SIR:

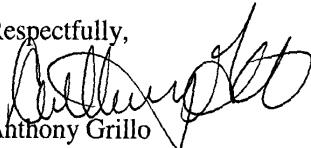
Please make of record the attached six (6) sheets of formal drawings in the above-identified application.

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D. C. 20231 on 3/22/01 (Date of Deposit)
Maureen Sailesh Chittipeddi Date

Group Art Unit 2814

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Respectfully,


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Agere Systems Inc.

Date: 3/22/01

Attachment